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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/060,750	01/30/2002	Robert J. Devins	BUR9-2001-0016-US1	7058

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/060,750	DEVINS ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-34 of U.S. Application 10/060,750 filed on 01/30/2002 are presented for examination.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. The prior art used for these rejections is as follows:

5. Blaner, B. et al. "An Embedded PowerPC™ SOC for Test and Measurement Applications." 13th Annual IEEE Int'l ASIC/SOC Conf., 2000. Sept. 13-16, 2000. pp.204-208. (Henceforth referred to as "**Blaner**").

6. Devins et al., U.S. Patent 6,487,699. (Henceforth referred to as "**Devins**"). Examiner notes that the issued patent has a different inventive entity.

7. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

8. **Claims 1-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Blaner.**

9. In regards to Claim 1, Blaner teaches the following limitations:

1. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

a test bench external bus interface unit (EBIU) connected to said verification interface model, wherein said test bench EBIU is connected to a SOC EBIU within said SOC.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the

SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

10. In regards to Claim 2, Blaner teaches the following limitations:

2.The verification test bench system in claim 1, wherein said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

11. In regards to Claim 3, Blaner teaches the following limitations:

3.The verification test bench system in claim 1, wherein said SOC interface and said verification interface model are programmed by a test case running in said SOC.

(See Blaner, especially: p.205, "II. SOC Structure" and p.208, "E. Verification Testbench")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called***

the external bus master, to take ownership of the external bus and access attached memories."

Blaner also teaches (See "E. Verification Testbench". Emphasis added): "Wrap backs are utilized as much as possible, and behaviorals often contain hard-coded packet or stream data."

Examiner interprets that "Wrap backs" do not containing functioning processors, and therefore must rely on the SOC processor.

12. In regards to Claim 4, Blaner teaches the following limitations:

4.The verification test bench in claim 3, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

13. In regards to Claim 5, Blaner teaches the following limitations:

5.The verification test bench in claim 3, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU) controls up to eight banks of mixed types of memories*** and operates at one-half the PLB [processor local bus] clock frequency. ... Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories."

14. In regards to Claim 6, Blaner teaches the following limitations:

6. The verification test bench system in claim 1, wherein said verification interface model tests an operational capability of said SOC interface.

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench."

15. In regards to Claim 7, Blaner teaches the following limitations:

7. The verification test bench system in claim 1, further comprising at least one additional verification interface model connected to said test bench EBIU for testing additional types of SOC interfaces.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

16. In regards to Claim 8, Blaner teaches the following limitations:

8. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC.

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "Wrap backs are utilized as much as possible, and behaviorals often contain hard-coded packet or stream data."

Examiner interprets that "Wrap backs" do not containing functioning processors, and therefore must rely on the SOC processor.

17. In regards to Claim 15, Blaner teaches the following limitations:

15. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC, such that said SOC interface and said verification interface model are programmed by the same test case running in said SOC.

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "Wrap backs are utilized as much as possible, and behaviorals often contain hard-coded packet or stream data."

Examiner interprets that "Wrap backs" do not containing functioning processors, and therefore must rely on the SOC processor.

18. In regards to Claim 21, Blaner teaches the following limitations:

21. A method of testing a system-on-a-chip (SOC) interface of an SOC, said method comprising:

connecting a verification interface model to said SOC interface;

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

connecting a test bench external bus interface unit (EBIU) to said verification interface model;

connecting said test bench EBIU to a SOC EBIU within said SOC; and comparing said SOC interface with said interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification

of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

19. In regards to Claim 28, Blaner teaches the following limitations:

28. A program storage device readable by machine tangibly embodying a program of instructions executable by the machine to perform a method for testing a system-on-a-chip (SOC) interface of an SOC, said method comprising:

connecting a verification interface model to said SOC interface;

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

connecting a test bench external bus interface unit (EBIU) to said verification interface model;

connecting said test bench EBIU to a SOC EBIU within said SOC; and

comparing said SOC interface with said interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

20. Dependent Claims 2, 9, 16, 22, and 29 differ only in the limitations that they inherit from their parent claims. Therefore Claims 9, 16, 22, and 29 are rejected for the same reasons as claim 2, in combination with the rejections of their respective parent claims, which are recited above.

21. Dependent Claims 3, 10, 23, and 30 differ only in the limitations that they inherit from their parent claims. Therefore Claims 10, 23, and 30 are rejected for the same reasons as claim 3, in combination with the rejections of their respective parent claims, which are recited above.

22. Dependent Claims 4, 11, 17, 24, and 31 differ only in the limitations that they inherit from their parent claims. Therefore Claims 11, 17, 24, and 31 are rejected for the same reasons as claim 4, in combination with the rejections of their respective parent claims, which are recited above.

23. Dependent Claims 5, 12, 18, 25, and 32 differ only in the limitations that they inherit from their parent claims. Therefore Claims 12, 18, 25, and 32 are rejected for the same reasons as claim 5, in combination with the rejections of their respective parent claims, which are recited above.

24. Dependent Claims 6, 13, 19, 26, and 33 differ only in the limitations that they inherit from their parent claims. Therefore Claims 13, 19, 26, and 33 are rejected

for the same reasons as claim 6, in combination with the rejections of their respective parent claims, which are recited above.

25. Dependent Claims 7, 14, 20, 27, and 34 differ only in the limitations that they inherit from their parent claims. Therefore Claims 14, 20, 27, and 34 are rejected for the same reasons as claim 7, in combination with the rejections of their respective parent claims, which are recited above.

26. Claims 1-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Devins.

27. In regards to Claim 1, Devins teaches the following limitations:

1. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC.

The "external bus interface logic" in the "device is coupled to said system-on-chip device via a chip-external bus" that is claimed in claim 18 of the issued Devins patent is enabled in the specification of that patent in Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8. This corresponds to the "test bench external bus interface unit (EBIU)" claimed in claims 1, 8, and 15 of the instant application.

While the issued patent does not expressly teach that the "system-on-chip" device also uses an EBIU in order to connect to the test unit's EBIU,

Examiner finds this to be inherent because the two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This reasoning is especially relevant because the issued patent teaches (See col.4, lines 15-20):

> The external bus interface logic 202 is designed to direct signals received via connection 107 to the appropriate logical address, and to convert the particular bus protocol received into an internally-used format applicable to the command decode logic 203.

28. In regards to Claim 2, Devins teaches the following limitations:

2.The verification test bench system in claim 1, wherein said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

29. In regards to Claim 3, Devins teaches the following limitations:

3.The verification test bench system in claim 1, wherein said SOC interface and said verification interface model are programmed by a test case running in said SOC.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

30. In regards to Claim 4, Devins teaches the following limitations:

4.The verification test bench in claim 3, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

31. In regards to Claim 5, Devins teaches the following limitations:

5.The verification test bench in claim 3, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

32. In regards to Claim 6, Devins teaches the following limitations:

6. The verification test bench system in claim 1, wherein said verification interface model

tests an operational capability of said SOC interface.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

33. In regards to Claim 7, Devins teaches the following limitations:

7. The verification test bench system in claim 1, further comprising at least one additional verification interface model connected to said test bench EBIU for testing additional types of SOC interfaces.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

34. Independent Claims 8, 15, 21, and 28 are rejected on the same grounds as claim 1.

35. Dependent Claims 2, 9, 16, 22, and 29 differ only in the limitations that they inherit from their parent claims. Therefore Claims 9, 16, 22, and 29 are rejected for the same reasons as claim 2, in combination with the rejections of their respective parent claims, which are recited above.

36. Dependent Claims 3, 10, 23, and 30 differ only in the limitations that they inherit from their parent claims. Therefore Claims 10, 23, and 30 are rejected for the same reasons as claim 3, in combination with the rejections of their respective parent claims, which are recited above.

37. Dependent Claims 4, 11, 17, 24, and 31 differ only in the limitations that they inherit from their parent claims. Therefore Claims 11, 17, 24, and 31 are rejected for the same reasons as claim 4, in combination with the rejections of their respective parent claims, which are recited above.

38. Dependent Claims 5, 12, 18, 25, and 32 differ only in the limitations that they inherit from their parent claims. Therefore Claims 12, 18, 25, and 32 are rejected

for the same reasons as claim 5, in combination with the rejections of their respective parent claims, which are recited above.

39. Dependent Claims 6, 13, 19, 26, and 33 differ only in the limitations that they inherit from their parent claims. Therefore Claims 13, 19, 26, and 33 are rejected for the same reasons as claim 6, in combination with the rejections of their respective parent claims, which are recited above.

40. Dependent Claims 7, 14, 20, 27, and 34 differ only in the limitations that they inherit from their parent claims. Therefore Claims 14, 20, 27, and 34 are rejected for the same reasons as claim 7, in combination with the rejections of their respective parent claims, which are recited above.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273- 8300, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Paul L. Rodriguez 8/19/05

Primary Examiner
Art Unit 2125

Ayal I. Sharon

Art Unit 2123

August 19, 2005